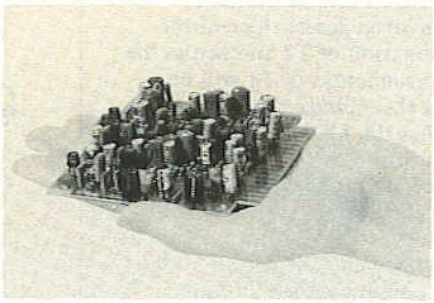
presence of significant harmonic interference from the base band during playback.

The synchronous detector compares the phases of the VCO and the input carrier signal, producing an output signal which accords with the condition of the input signal. This output signal is fed to the lock range controller which controls the PLL so that it is set to the condition most suitable to the input signal, giving a demodulated output which is compensated for carrier loss.

Figure 6 is a block diagram of a standard circuit using the CD4-392.

History of the CD-4 demodulator

Figure 7 is a photograph showing the progress made in CD-4 demodulators.



The CD4-1 is the first generation demodulator used when the CD-4 system was first released, the 4DD-5 is the second generation demodulator using the PLL IC and the TDM-18A is the third generation demodulator which incorporates the CD4-392 IC.

Figure 8 is a schematic diagram of the standard TDM-19A. The TDM-18A and the TDM-19A represent a significant step forward in the design and evolution of CD-4 playback hardware with their performance characteristics having been substantially improved. ◀

Figure 6. Block diagram of CD4 demodulator.

Figure 7. From left to right: the CD4-1, the 4DD-5 and the TDM-18A.

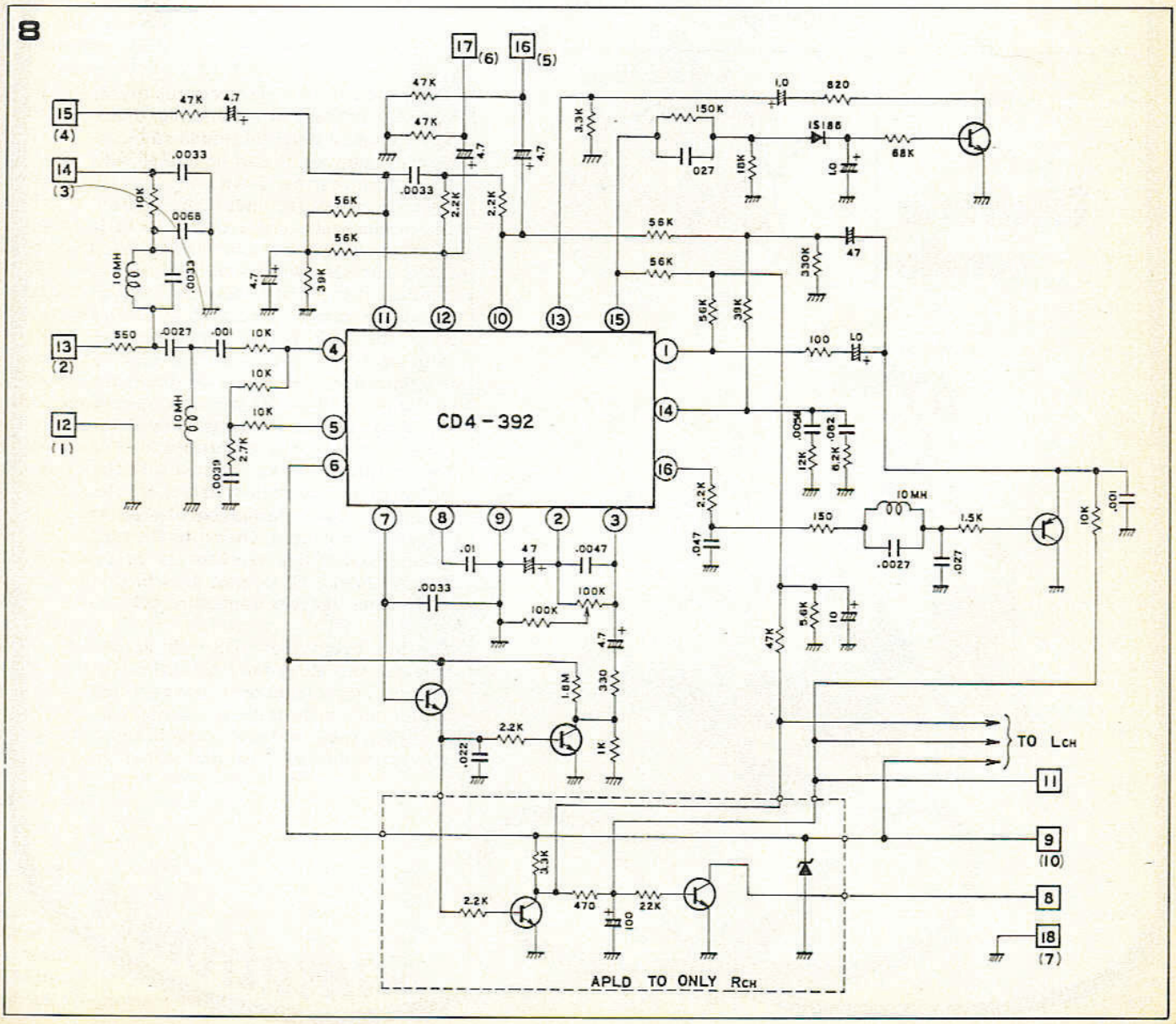



Figure 8. A complete CD-4 demodulator using the CD4-392 (one channel shown).