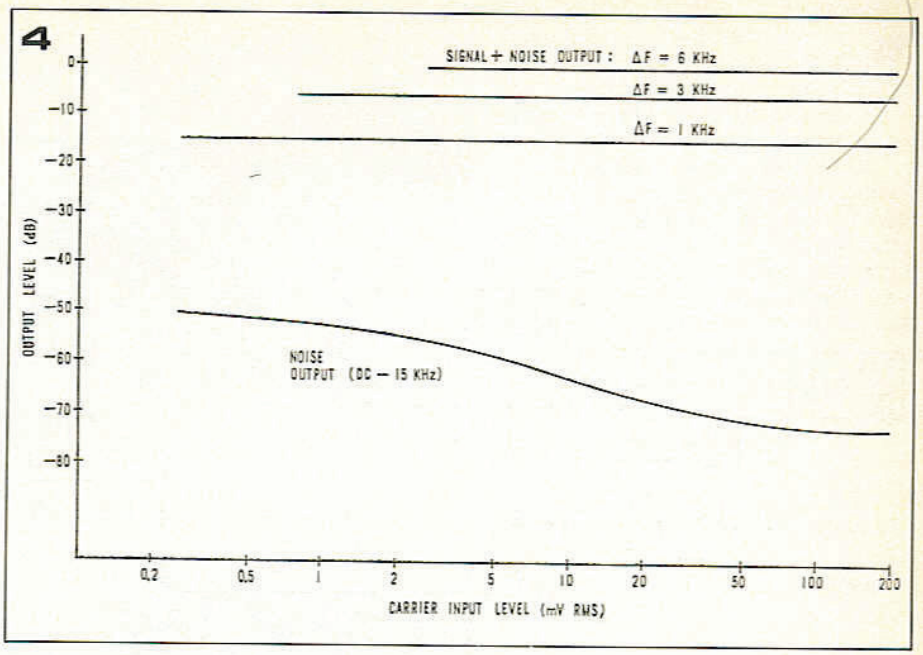
Figure 1. Pin configuration of CD4-392 IC.

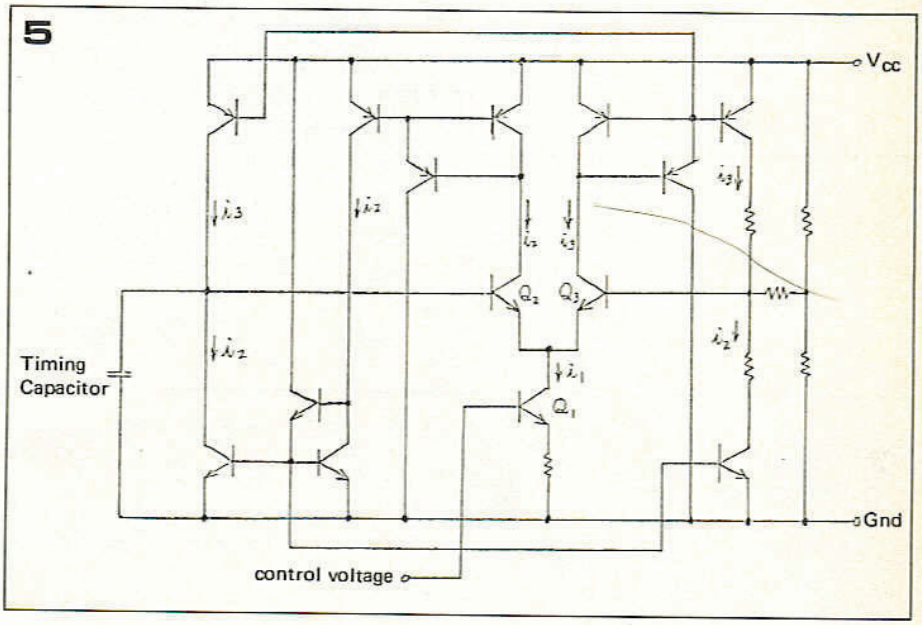
Figure 2. Block diagram of demodulator using the CD4-392 IC.

Figure 3. AC/DC lock range characteristics of PLL.

Figure 4. Quieting curve of carrier recovery system.

Figure 5. Schematic diagram of voltage controlled oscillator.





which are of the same value are applied to a capacitor connected to the base of transistor Q2. The pair of transistors are switched ON and OFF in response to the charging and discharging of the capacitor via the current mirror circuits connecting the pair of transistors. The control signal controls the oscillation frequency of the linear voltage controlled oscillator.

Circuits external to the IC

The IC has been designed so that a number of approaches to ancillary circuitry can be accommodated.

1. Band-pass and low-pass filtering.
   Either passive LCR or active RC devices can be used.
2. RIAA Equalization
   Normally, the RIAA circuit is divided into two sections, LF boost and HF roll-of, with the feed to the carrier recovery system taken before the HF roll-off. However, as the carrier can be limited by up to 50 dB in this IC, it is possible to take the feed to the carrier recovery system after the RIAA equalizer.
3. ANRS System
   ANRS is an encode-decode noise reduction system and the parameters in playback must match those used in the recording system. Splitting the ANRS into two blocks facilitates a number of approaches to the tailoring of the dynamic characteristics of the ANRS to those desired.
4. Carrier loss compensation
   Carrier loss can result from self-erasure of the HF signal during the cutting process as well as from the

CD4·392 DEMODULATOR IC CHIP PATTERN